Feature Detection Plugins Speed-up by OmpSs@FPGA

Nicola Bettin
Daniel Jimenez-Gonzalez
Xavier Martorell
Pierangelo Nichele
Alberto Pomella
nicola.bettin@Vimar.com, pierangelo.nichele@Vimar.com, alberto.pomella@Vimar.com
djimenez@ac.upc.edu, xavim@ac.upc.edu

Introduction

Vimar S.p.A.:

- Italian company from Marostica (VI)

Vimar S.p.A. develops and manufactures devices and systems for Home and Building automation:

- Wiring devices
- Smart Home devices
- Video Door Entry Systems
- Access control
- Multi room audio
- Comfort and HVAC
- Security / TVCC
- …

Agenda

AXIOM Horizon2020 European Project

AXIOM main goals

The AXIOM BOARD and the AXIOM Software layer

OmpSs: Programming model

Cyber-Physical Systems (CPS) and Smart Home

Feature detection and extraction plugins

Exploration: Cepstrum Analysis Plugin

- GStreamer application
- GStreamer & OmpSs@FPGA

Conclusion

AXIOM Horizon2020 European Project

VIMAR group
energia positiva

AXIOM

http://www.axiom-project.eu

ICT-01-2014 GA 645496

Agile, eXtensible, fast I/O Module for the cyber-physical era

PROJECT ID: 645496

Agile, eXtensible, fast I/O Module for the cyber-physical era

- Project partners:
  - VIMAR | Home automation, electrical equipment (Domotic)
  - Herta Security | Cutting edge facial recognition solutions (Videosurveillance)
  - BSC | Barcelona Supercomputing Center (OmpSs)
  - Evidence | Embedded software development (LinuxOS + RunTime)
  - FORTH | Foundation for Research and Technology – Hellas (Interconnection)
  - SECO | Embedded Creators (Which will actually build the computer)
  - UNISI | Università degli Studi di Siena (Coordination, Evaluation, Dissemination, Exploitation)

University of Siena (Coordinator Partner)

Barcelona Supercomputing Center
Centro Nacional de Supercomputación

EVIDENCE EMBEDDING TECHNOLOGY

herta security

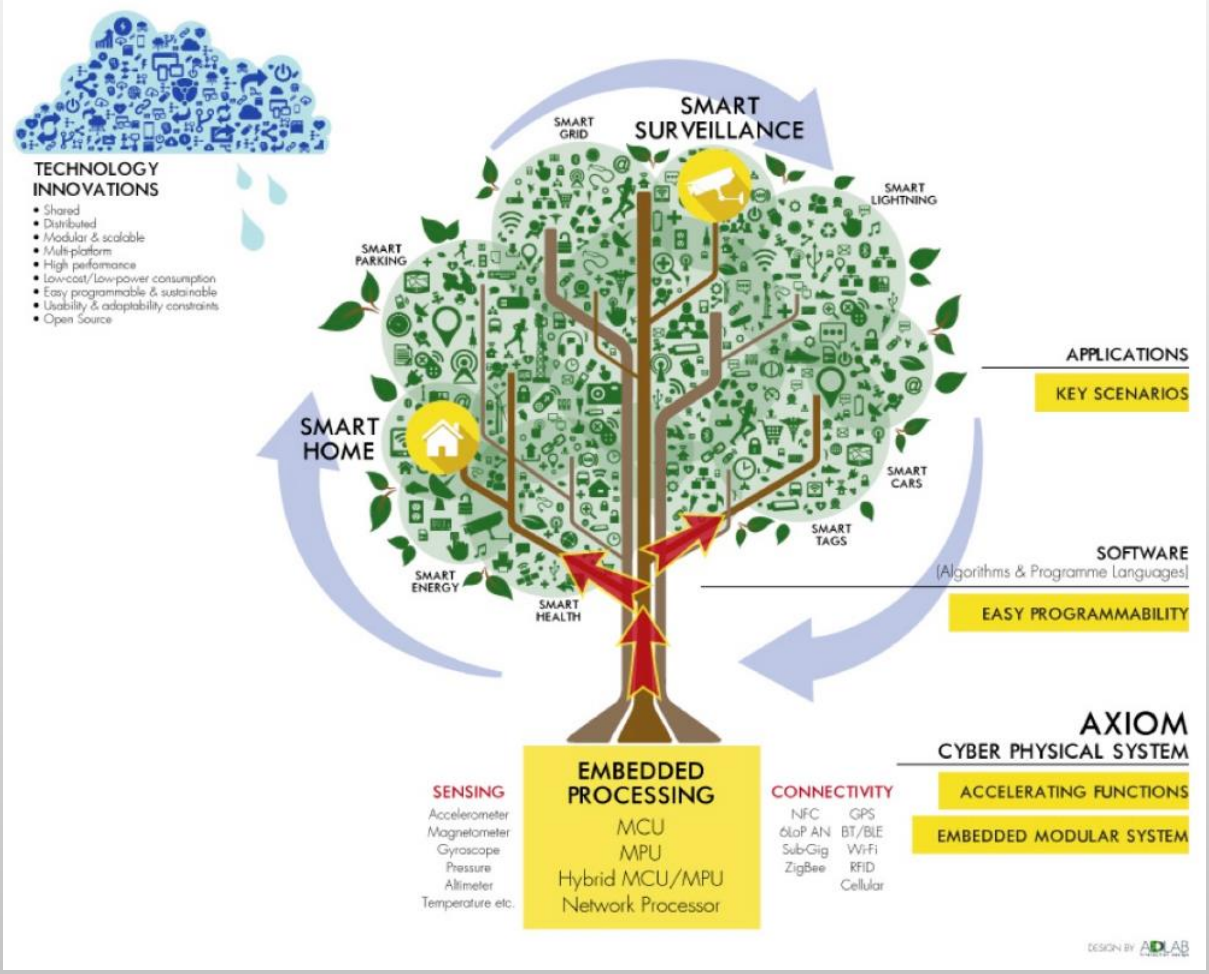
FORTH Institute of Computer Science

SECO

VIMAR energia positiva

AXIOM Horizon2020 European Project

We are entering the Cyber-Physical Era where natural interactions are required between humans and machines



Main goals of AXIOM:

- Realize a small board that is flexible, energy efficient and scalable
- easy programmability of multi-core heterogeneous architectures (CPU+ FPGA) and multi-board architectures.
- Use and develop Open-Source software to manage the board
- Allow real-time thread scheduling
- Contribute to Standards

The AXIOM board and AXIOM software layer

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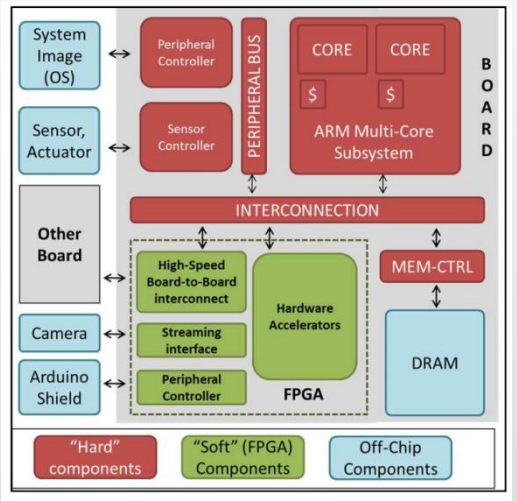
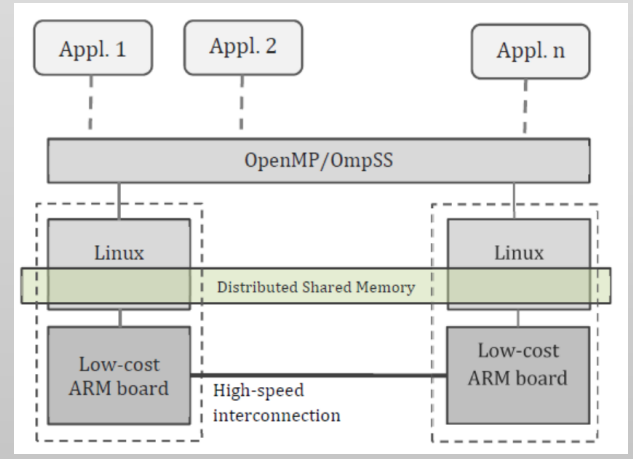
HW

- SoC + FPGA: Xilinx Zynq Family
  - ➢ Integrate on the same chip multiple cores ARM and FPGA.
- The FPGA is used to:
  - ➢ Implement custom accelerators to speedup algorithms and data processing
  - ➢ Implement high-speed connections for board-to-board communication (with low cost cable)



SW

- Linux-based OS and Linux Device Driver
- Programming model OmpSs
- Portions of applications on FPGA
  - – OmpSs@FPGA: Map tasks on the HW resources.
- At cluster level (multi-board):
  - – OmpSs@Cluster: Map tasks on boards cluster



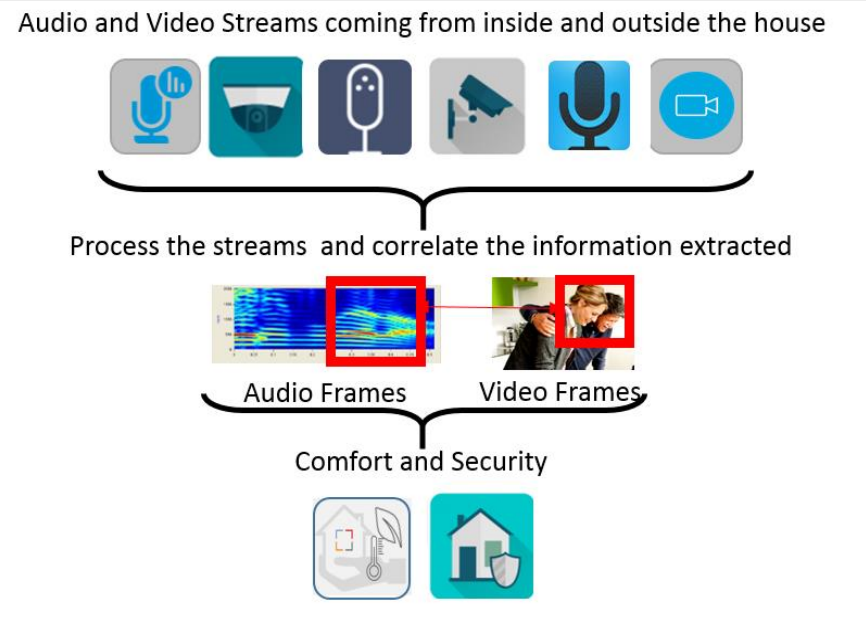
OmpSs : Programming Model

- "**OmpSs** is an effort to integrate features from the StarSs programming model developed by BSC into a single programming model. In particular, **our objective is to extend OpenMP with new directives to support asynchronous parallelism and heterogeneity** (devices like GPUs)." **from OmpSs website https://pm.bsc.es/ompss*

- **OmpSs is based on:**
  - **Mercurium compiler:**
    - to understand OmpSs directives to transform the code to run with *asynchronous* parallelism and *heterogeneity.*
  - **Nanos++:**
    - a runtime designed to serve as runtime support in parallel environments.

Cyber-Physical Systems and smart home

The **Cyber-Physical Systems (CPS)** have to permit a rapid and close interaction between system and human.



The **smart home is Cyber-Physical Systems:** a space where humans and the environment interact.

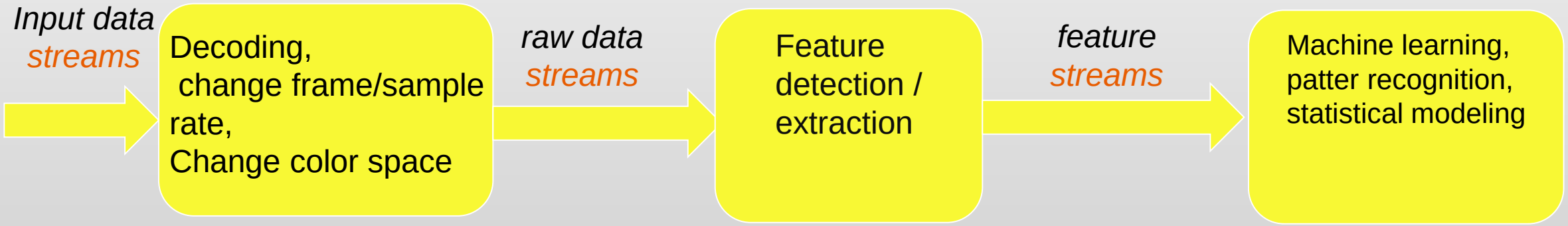
To enable a natural interaction between the user and the smart home, we need to **extract information** from multimedia streams recorded inside and outside the house.

The **GStreamer framework** with his capability to manage the multi-media streams is a good candidate to be used into CPSs inside the Smart Home.

Feature detection and extraction plugins

To extract information from multimedia streams machine learning methods are used.

In all these methods, the input data are processed to be transformed in a set of features (features detection and extraction).



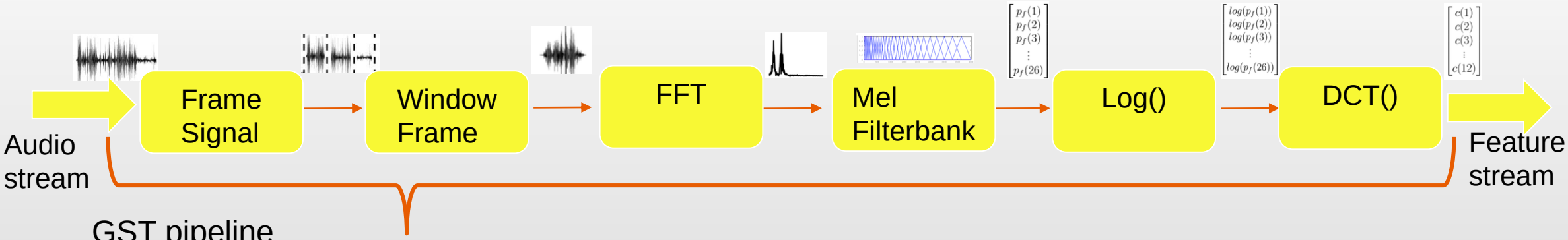
Features detection/extraction from audio stream:

- Cepstral analysis: Mel Frequency Cepstral Coefficients (MFCCs)

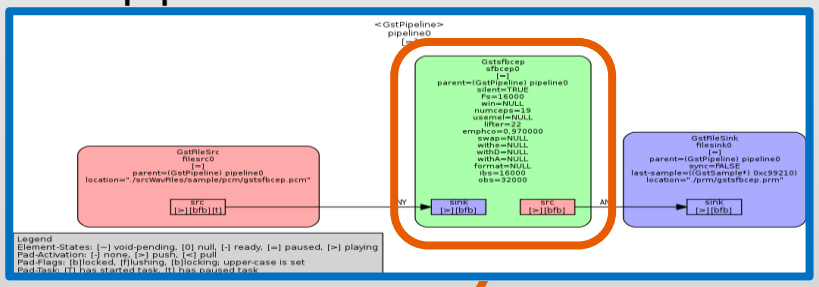
Features detection/extraction from video stream:

- Edge detection: Canny, Sobel

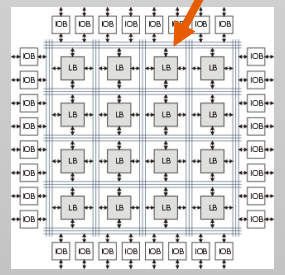
Exploration: Cepstrum Analysis Plugin



GST pipeline



OmpSs@FPGA



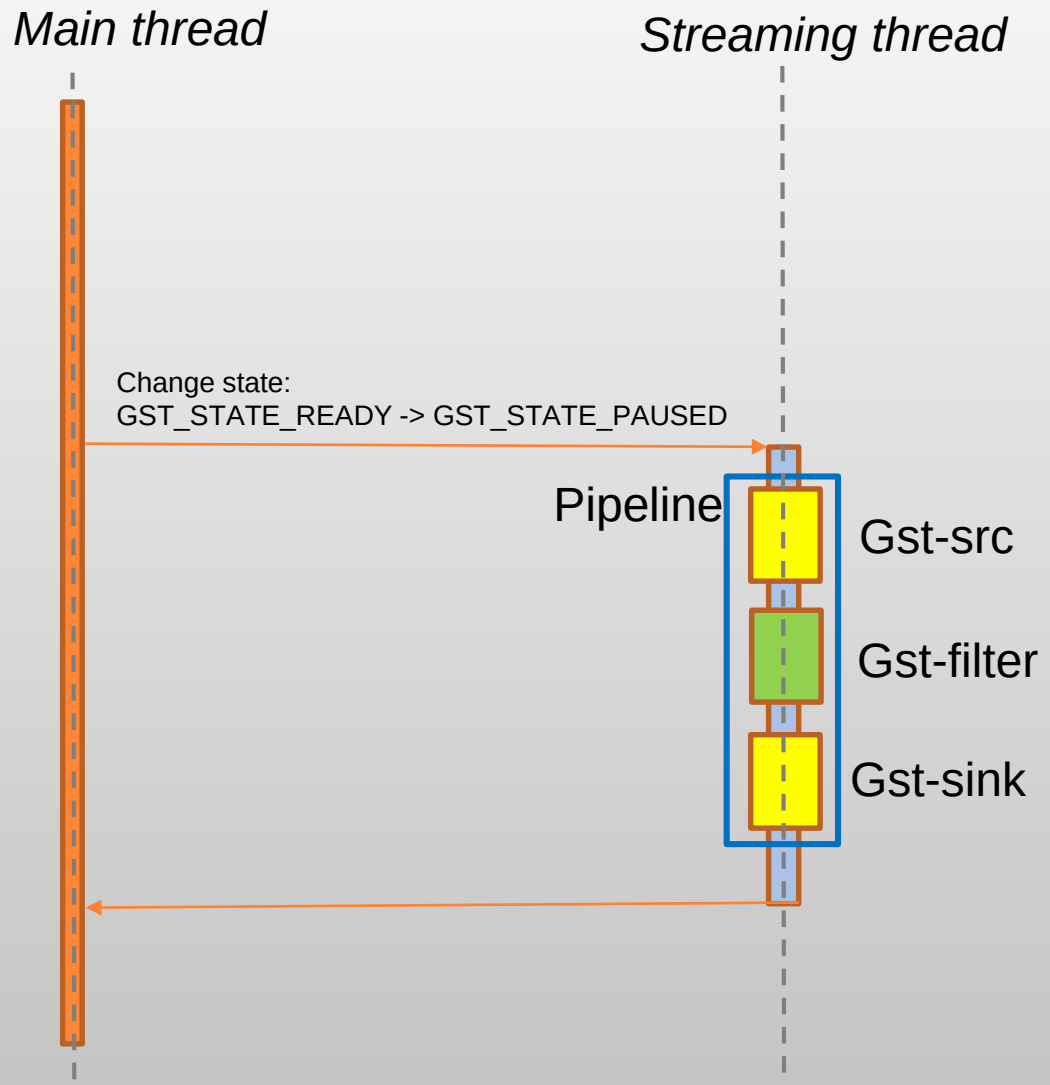
FPGA resources

MAIN STEPS:

1. Develop a GStreamer plugin for feature extraction
2. Parallelize the feature extraction plugin with OmpSs Programming Model
3. “Mapping” the OmpSs tasks on the HW resource in FPGA.

A crucial point is to leave the possibility of mixing in the pipeline “standard” plugins and "OmpSs" plugins.

GStreamer & OmpSs



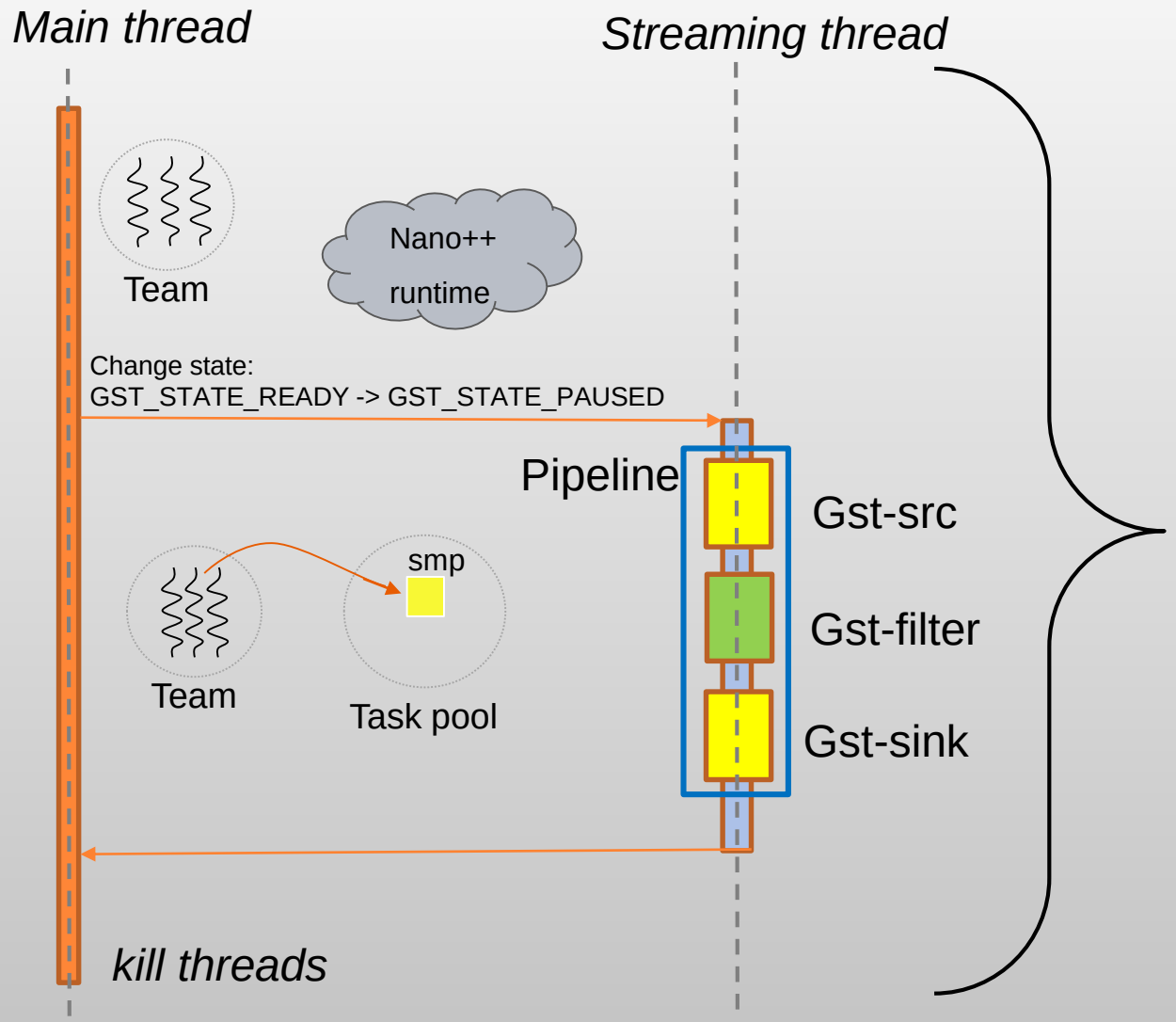
FIRST TEST:

Parallelization of features extraction plugin

- Compile with OmpSs directives only the features extraction plugin

☹ Low performance because OmpSs uses a thread-pool model.. overhead to create and destroy threads

GStreamer & OmpSs



SECOND TEST:

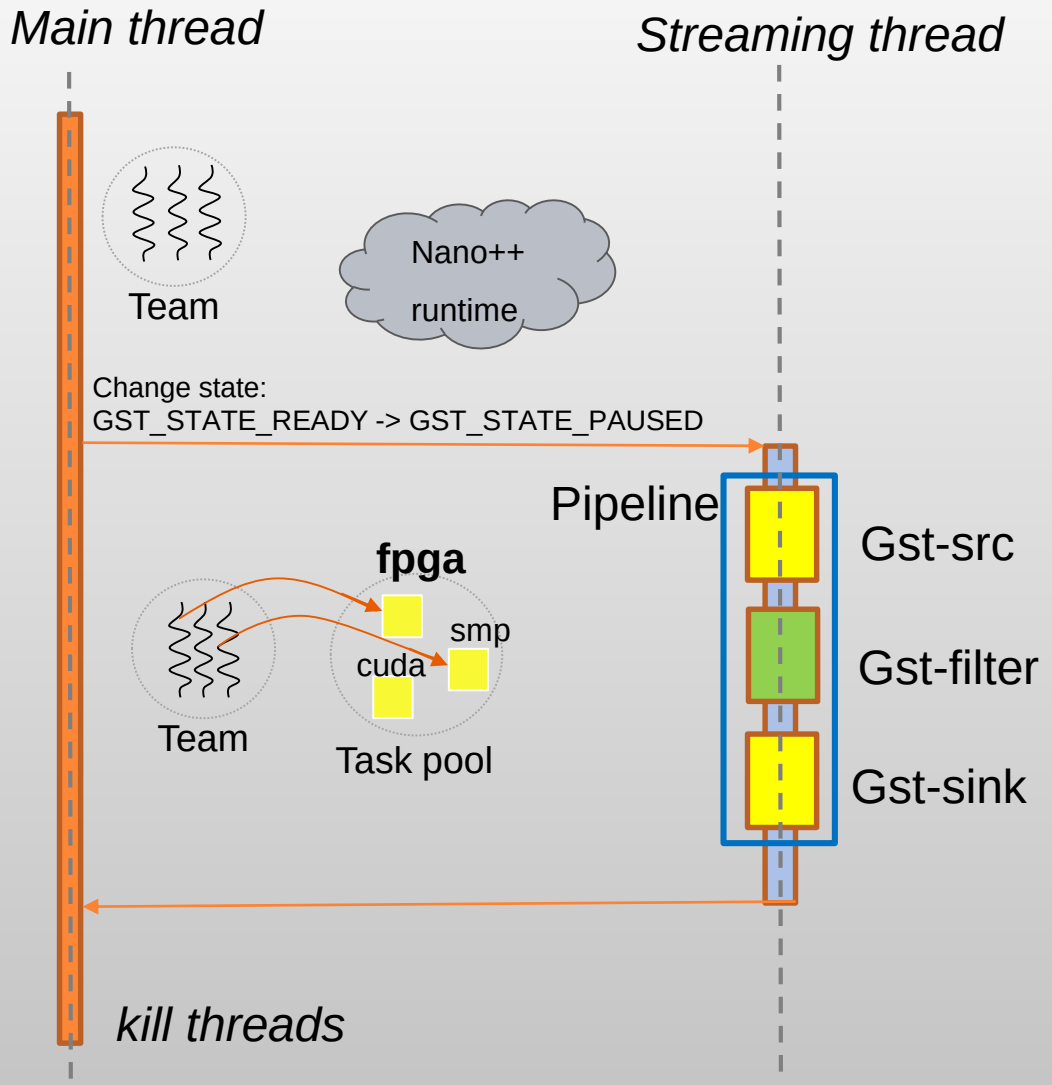
Parallelization of features extraction plugin + GST Application

- Compile with the OmpSs directive the features extraction plugin and the GST application.

☺ Better performance because OmpSs creates all the threads on application startup and uses these to process the tasks in the feature extraction plugin….

☺ …and OmpSs can use these threads in all the plugins that have the OmpSs directives in the pipeline

Next Steps



NEXT STEPS:

- Introduce the OmpSs directive to process the features extraction plugin in FPGA
- Evaluate the performance increase due to the parallelization and HW acceleration

Conclusion

1. We develop a features detection and extraction plugins

2. We demonstrated that OmpSs Programming Model can be used to parallelize the GStreamer application and plugins

3. Next steps: Speedup GST plugins inside the FPGA on AXIOM board and evaluate the performance increase

Update

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THANKS!

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Pierluigi Passera
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Reference

- https://pm.bsc.es/ompss
- https://gstreamer.freedesktop.org/data/doc/gstreamer/head/manual/manual.pdf
- https://gstreamer.freedesktop.org/data/doc/gstreamer/head/pwg/pwg.pdf
- http://www.axiom-project.eu/
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- http://www.sciencedirect.com/science/article/pii/S0141933116300850